lower impurity concentration than the n^+ source region **240**, effectually shortens the length of a channel **221** occurring in an upper region of the p-type body **220**.

[0019] An n^- second impurity region **242** is disposed between the channel **221** and the n^- extended drain region **230** on the surface of the n^- semiconductor substrate **200**. The n^- second impurity region **242** has a lower impurity concentration than the n^- semiconductor substrate **200**. Thus, there is no falloff of the impurity concentration in the channel **221** toward the n^- second impurity region **242**. An end portion of the n^- second impurity **242** may overlap an end portion of the channel **221**, in which case the channel length becomes even shorter.

[0020] An n^+ drain region **250** is disposed on the n^- extended drain region **230**. A gate stack is formed atop the channel **221** by a sequential forming of the gate isolating layer **260** and gate conducting layer **270**. Spacers **280** are formed on the sidewalls of the gate conducting layer **270**. The structure is completed by a double diffusion process in which a first ion implantation process is carried out before the gate spacer layer **280** is formed, and a second ion implantation process is carried out after the gate spacer layer **280** is formed. The n^+ source region **240** and the n^+ drain region **250** are electrically connected with a source electrode S and a drain electrode D, respectively, using general wiring formation techniques.

[0021] **FIG. 4** shows the relative impurity concentrations with respect to the channel of the LDMOS transistor of **FIG. 3**. For example, the n^+ source region **240** exhibits an impurity concentration curve A**2**, which is relatively high and decreases toward the n^- first impurity region **241**. The n^- first impurity region exhibits an impurity concentration curve B**2**, which is lower but shows a uniform ion distribution. The channel **221** in the p-type body **220** exhibits an impurity concentration curve C**2**, which also shows a fairly uniform ion distribution. The n^- second impurity region **242** exhibits an impurity concentration curve D**2**, which shows a very uniform ion distribution.

[0022] The uniform ion distribution of the channel **221** in the p-type body **220** is due to the n^- second impurity region **242**, which has a lower concentration than the n^- semiconductor substrate **200**, is disposed between the channel and the n^- extended drain region **230**. Thus, the impurity concentration of the channel **221** shows a very nearly uniform distribution even near the n^- second impurity region **242**.

[0023] Accordingly, in an LDMOS transistor of the present invention, a first impurity region surrounds a source region, thereby reducing the length of a channel occurring in a body. In addition, first and second impurity regions are disposed at either side of the channel, so that an impurity concentration shows a uniform ion distribution. As a result, channel length can be reduced, a sufficient breakdown voltage can be maintained, and an on-resistance characteristic can be improved.

[0024] It will be apparent to those skilled in the art that various modifications can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention covers such modifications provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A lateral double-diffused MOS transistor, comprising:

a drift region having a first conductivity;

a body having a second conductivity, said body being disposed in the drift region and having a channel thereon; and

a source region having the first conductivity, said source region being disposed within said body and having an upper region surrounded by a first impurity region having the first conductivity.

2. The lateral double-diffused MOS transistor according to claim 1, wherein the first impurity region has a lower impurity concentration than that of said source region.

3. The lateral double-diffused MOS transistor according to claim 1, further comprising:

a second impurity region having the first conductivity, said second impurity region being disposed between the channel and an extended drain region.

4. The lateral double-diffused MOS transistor according to claim 3, wherein said second impurity region has an impurity concentration lower than that of said drift region.

5. The lateral double-diffused MOS transistor according to claim 1, wherein the first conductivity is n-type and wherein the second conductivity is p-type.

6. The lateral double-diffused MOS transistor according to claim 1, wherein said drift region is formed by a semiconductor substrate having the first conductivity.

7. The lateral double-diffused MOS transistor according to claim 1, further comprising:

an extended drain region having the first conductivity, said extended drain region being disposed in said drift region and separated from said body;

a drain region having the first conductivity, said drain region being disposed in said extended drain region; and

a gate isolating layer and a gate conducting layer sequentially formed atop the channel occurring in said body.

8. A lateral double-diffused MOS transistor, comprising:

a first conductive type drift region;

a second conductive type body disposed on the drift region and defining a channel thereon;

a first conductive source region disposed on the body;

a first conductive type first impurity region surrounding the source region on the body;

a first conductive type extended drain region that is separated from the body;

a first conductive type drain region disposed on the extended drain region; and

a gate isolating layer and a gate conducting layer sequentially disposed on the channel.

9. The lateral double-diffused MOS transistor according to claim 8, wherein the first conductive type extended drain region is separated from the body by a predetermined distance on the drift region.

10. The lateral double-diffused MOS transistor according to claim 8, wherein the channel on the body surrounds the first conductive type first impurity region.